IETE Journal of Research

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/tijr20

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To cite this article: Priyanka Tyagi, Sanjay Kumar Singh & Piyush Dua (2023) Ultra-Low Power 8-Transistor Modified Gate Diffusion Input Carbon Nano-Tube Field Effect Transistor Full Adder, IETE Journal of Research, 69:8, 5518-5531, DOI: 10.1080/03772063.2021.1962746

To link to this article: https://doi.org/10.1080/03772063.2021.1962746

IETE JOURNAL OF RESEARCH
2023, VOL. 69, NO. 8, 5518–5531
https://doi.org/10.1080/03772063.2021.1962746

Ultra-Low Power 8-Transistor Modified Gate Diffusion Input Carbon Nano-Tube Field Effect Transistor Full Adder

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ABSTRACT

An ultra-low power 8-Transistor Modified Gate Diffusion Input (MGDI) Carbon Nano Tube Field Effect Transistor (CNTFET) Full Adder (FA) has been presented in this paper. The proposed 8-T MGDI CNTFET Full Adder outperforms other adders in terms of Power Consumption, Propagation Delay and the PDP at different levels of Power Supply and Temperatures. The power consumption of the proposed 10 nm CNTFET 8-T MGDI Full Adder at 27°C is 1.96 nW. The proposed CNTFET FA exhibits 60.32% improvement in Power Consumption when compared to the existing 10 nm FINFET 8-T MGDI Full Adder. The propagation Delay of the proposed FA is 42.16 ps and an improvement of 57.68% is noticed over the existing FA. The Power Delay Product of the proposed 10 nm CNTFET 8-T MGDI FA is 82.63 $\times$ 10^{-21} Jules, whereas the PDP of the 10 nm FINFET 8-T MGDI FA is 492.07 $\times$ 10^{-21} Jules. The PDP of the proposed 10 nm CNTFET 8-T MGDI Full Adder exhibits 83.21% improvement when compared to the 10 nm FINFET 8-T MGDI FA.

KEYWORDS

CNTFET; FINFET; Full Adder; MGDI; Ultra-low power; 8-Transistor Full Adder

1. INTRODUCTION

In the modern digital electronics the 1-bit full adder is a basic block for arithmetic units, memory units and different logical operations. The full adder cell is deployed in other circuits such as multipliers and different kinds of adders, such as RippleCarry Adder (RCA), Carry Save Adder (CSA), *etc*. The above-mentioned adders are used in various data path elements to perform different arithmetic operations. Hence, a novel fast, low-power, and low area 8- T MGDI full adder cell has been proposed using10 nm CNTFET in this paper.

The regular Metal–Oxide Semiconductor Field Effect Transistors (MOSFETs) come across serious difficulties at the nano-scale region, such as the huge leakage current, short-channel effects, process-corner variations, *etc* [1,2]. Consequently, a few innovative technologies had emerged for nano-electronics in the recent years. Carbon Nano Tube Field Effect Transistor (CNTFET) is the guaranteed technology instead of MOSFET devices. CNTFET offers great flexibility to design low-power and high-performance circuits and CNTFET has very low off-current [3]. The performance and efficiency of the proposed CNTFET FA has been analyzed across all Process-Voltage-Temperature (PVT) corners. Mostly single-wall carbon-nanotubes (SWCNTs) are used as channels in CNTFET. Depending upon the chirality vector CNTs can be work as semiconductors, metals or conductors [4]. High Speed and Low Power CNTFET approximate FA Cell for Image Processing Application has been implemented [5].

Carbon nanotubes (CNTs) are most promising onesin today's electronic world. CNT has the 1D quasi-structure. The unique properties of the CNTs led their use in nano-applications. The properties of CNTs are determined by their fabrication process [6]. CNTs, mainly SWCNTs, are the up-growing material for the electronic field. SWCNTs are going to take the place of the silicon in the coming years. CNTFETs are going to replace the silicon-based transistors [7]. The main advantage of the CNT is that it reduces the amount of material used in the fabrication process. The conventional silicon transistor requires the bulk of silicon. CNT reduces the amount of the material used for the fabrication of the transistors [8]. The properties such as high mobility of the carrier, low capacitance and the nanometer channel length promote the use of CNTs for ultra-high speed applications [9]. CNFETs are used to design low power and high performance circuits [10,11]. CMOS devices have large leakage currents and short-channel effects [10–12]. SWCNT can act as a conductor (metal) and as a semiconductor as well [11,12]. Figure 1 shows the gate-all-around structure of CNTFET.

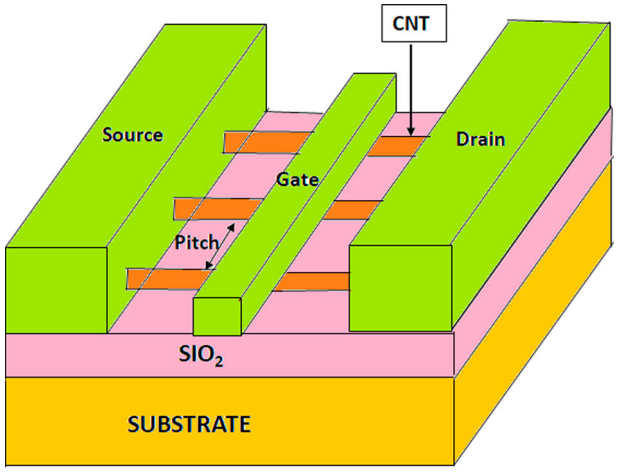

Figure 1: 3D structure of the CNTFET model

The remainder of the research article is structured as follows. Related research work on CNTFET-FA has been discussed in Section 2. Design of the proposed CNTFET-FA cell has been offered in Section 3. Simulation outcomes have been discussed in Section 4. Finally, Section 5 concludes the paper.

2. RELATED RESEARCH WORK

Different implementations of full-adder cells are available in the literature [12–20]. Few full adders were employed with MOSFETs and CNTFETs. The complementary-pass-transistor logic FA [14] was implemented using a 32-transistor. The CNTFET-FA implemented by the majority function is presented in [15]. Complementary-CMOS (C-CMOS) FA [16] using 28-transistors was implemented.

The multi-output-dynamic FA [17] using 21-transistors was proposed. Transmission-gates [18] using 20-transistors were presented. A high-speed capacitor-inverter-based CNTFET-FA is presented [19]. Energy-efficient CNTFET-FA [20] based on majority function, 8-transistors and 5-capacitors is offered. 14-transistor CNTFET-FA [21] was implemented. A dynamic-CNTFET-FA cell [22], 8 T MGDI CMOS Full Adder cell [23] and 8 T MGDI FINFET Full Adder [24] were implemented.

High-Efficient Full Adder Circuit was implemented by Seyedehsomayeh [25]. CNTFET-based Low Power Ternary Full Adder was discussed by F. Jafarzadehpour *et al.* [26]. CNTFET-based Quaternary Full Adder was implemented by Krishna Chaitanya *et al.* [27]. Carbon nanotube FET-based multi-digit adder was implemented to optimize the parameter such as power and delay by B. Srinivasu *et al.* [28]. A CNTFET Ternary Full adder for Carry Generation Circuit to improve the performance of the design was implemented by Subhendu Kumar Sahoo *et al.* [29].

A full adder cell is designed using a XOR–XNOR gate and a multiplexer circuit [30]. The design has the 23 transistors. The sum was designed by the transmission gate technique and the carry output design was implemented by the GDI technique. This adder is used to implement the 4:2 compressors.

The proposed full adder is implemented using 20 transistors [31]. The high-performance design is applicable for different carry adder formats. The 14T high-speed GDI full adder is implemented with two different strategies [32]. A power-efficient 10 T full adder was designed using majority of NOT function [33].

3. PROPOSED RESEARCH WORK

The CNTFET has very less effect of temperature on the threshold voltage, but the threshold voltage of the MOSFET decreases drastically with temperature. So, the leakage power in MOSFET circuits will be huge at high temperature and the leakage power increases exponentially with the rise in temperature. But, the impact of the temperature on the leakage power of the CNTFET is very minimal and it increases gradually with the rise in temperature. Hence the CNTFET circuit exhibits excellent Power, Performance and Area (PPA) optimization.

An ultra-low power 8-Transistor Modified-Gate-Diffusion-Input (MGDI) Carbon-Nano-Tube-Field-Effect-Transistor (CNTFET) Full Adder (FA) has been presented in this paper. The proposed CNTFET Full Adder has been implemented using the 10 nm CNTFET model and "10" Carbon Nano Tubes are used as channels under the gate to conduct the current from the source to drain. The performance metrics of the proposed 8-T MGDI CNTFET FA have been compared with those of the existing 8-T MGDI FINFET FA.

The proposed 8-T MGDI CNTFET FA consumes very less power because of the proposed structure and the Full Adder is operated with 0.5 V as the power supply. Power supply voltage is 0.5 V because the threshold-voltage of CNTFET is in terms of microvolts. Hence the switching speed of the proposed circuit is not affected. Moreover, the low power supply provides very good optimization in the power consumption of the proposed circuit because of the negligible amount of parasitic capacitance of the proposed CNTFET models. Hence the proposed 8-T MGDI CNTFET FA outperforms well by means of the

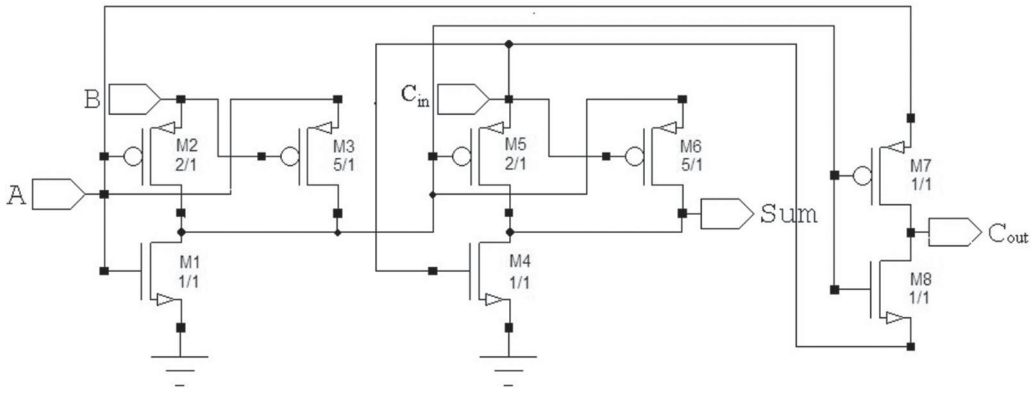

Figure 2: Schematic diagram of 8-T MGDI FINFET full adder [24]

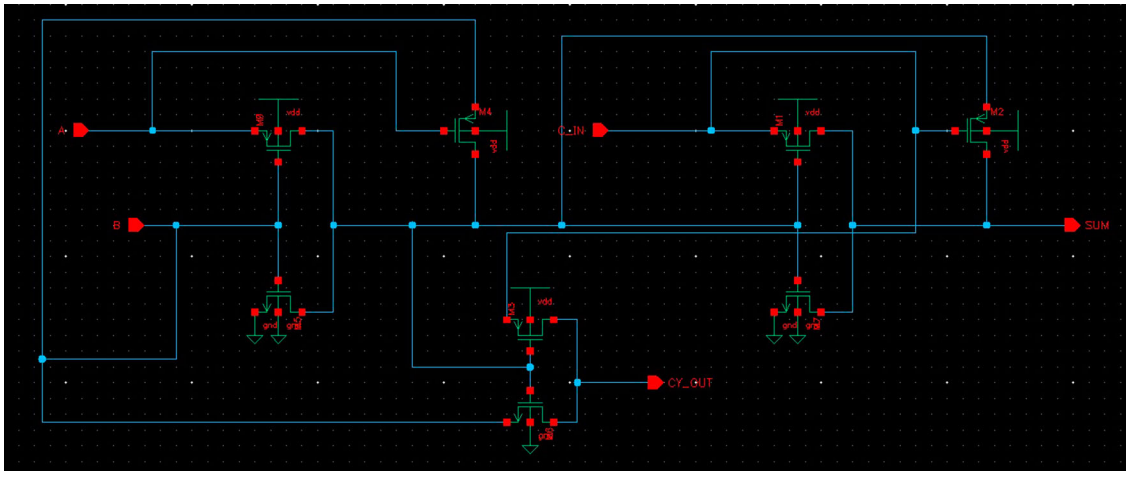

Figure 3: Schematic diagram of the proposed 8 T MGDI CNTFET FA

energy requirement, delay and PDP. So, the overall performance of the proposed FA is excellent when compared with the existing Full Adder designs.

Schematic diagram of the existing 8-T MGDI FINFET-FA has been displayed in Figure 2.

The existing 8-T MGDI FINFET FA circuit was implemented using a 10 nm FINFET library and the supply-voltage is 0.7 V. Schematic of the proposed 8-T MGDI CNTFET FA has been shown in Figure 3. The proposed 8-T MGDI CNTFET FA schematic diagram has been drawn using 10 nm N-CNTFET and P-CNTFET models in Cadence Schematic Composer Tool in Virtuoso Analog Design Environment.

The Test Bench of the proposed CNTFET-FA is displayed in Figure 4. The power supply voltage is 0.5 V. Pulse signals are given to the input terminals "A", "B", "C_IN" to generate all possible "8" combinations to the adder. The voltage level of the inputs is also 0.5 V. Transient analysis in Cadence is used to analyze the performance metrics of the proposed 8-T MGDI CNTFET-FA. The Truth-table of the FA is listed in Table 1. Input out waveforms of the proposed Full Adder is shown in Figure 5.

Table 1: Truth table of a full adder

Input-A	Input-B	Input-C_IN	SUM	CY_OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. SIMULATION RESULTS AND DISCUSSION

The proposed 8-T MGDI CNTFET FA has been implemented using 10 nm N-CNTFET and P-CNTFET models in the Cadence Schematic Composer Tool in Virtuoso Analog Design Environment.

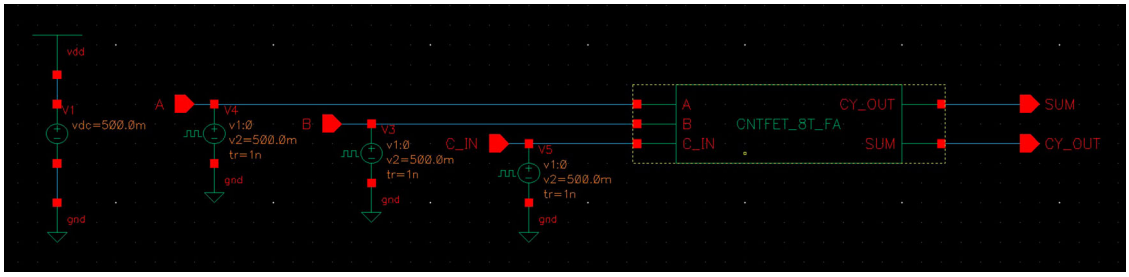

Figure 4: Test bench of the proposed 8 T CNTFET FA

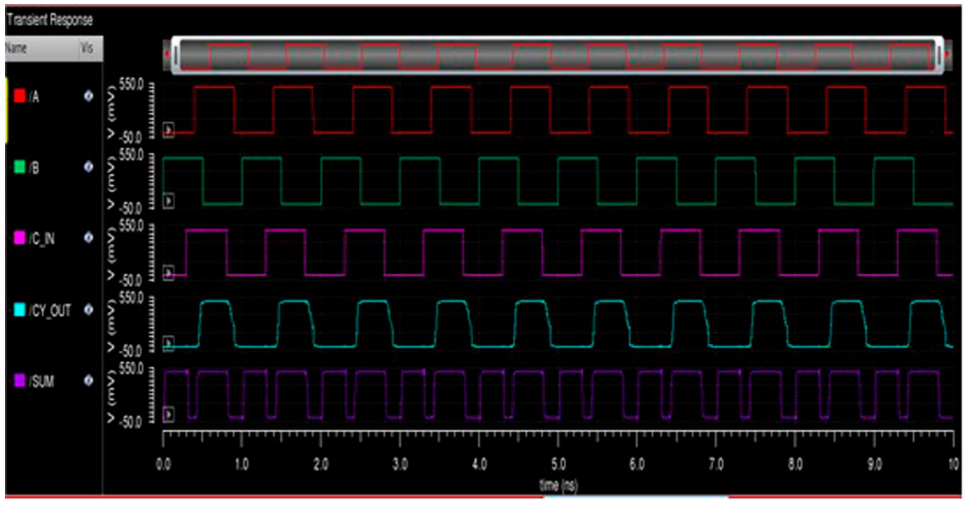

Figure 5: Input–output waveform of the proposed 8-T MGDI CNTFET

Table 2: Simulation parameters of the proposed circuit

Parameters	Values/Description
Technology Node	10 nm CNTFET
Length of the CNT	10 nm
Width of the CNT	1 µm
No of Carbon Nano-Tubes	10
Power Supply	0.5 V
Range of Power Supply	0.4 to 1.0 V
Simulation Temperature	27°C
Range of Temperatures	−25°C to 125°C
Analysis	Transient

Table 3: Power supply variations vs. power consumption @ 27°C

Power Supply V_{dd} (V)	8 T MGDI CNTFET FA (10 nm) [Proposed] Power (nW)	8 T MGDI FINFET FA (10 nm) [20] Power (nW)
0.4	0.98	3.12
0.5	1.96	4.94
0.6	3.04	7.82
0.7	4.51	11.74
0.8	6.43	16.86
0.9	8.86	23.34
1.0	11.93	31.28

The length of the Carbon Nano Tube channel is 10 nm and "10" Carbon Nano Tubes are under the gate to conduct the current from the Source terminal to the Drain terminal. The simulation parameters have been listed in Table 2.

Supply Voltage is 0.5 V and the simulation temperature is 27°C. Transient analysis in Cadence is used to analyze the performance metrics of the proposed 8-T MGDI CNTFET FA. The performance metrics, such as Power Consumption, Propagation Delay and the Power Delay Product, are measured and analyzed. The impact of the variation in the power supply on power consumption of the proposed 8-T MGDI CNTFET FA and the existing 8-T MGDI FINFET FA is listed out in Table 3.

The power supply is varied from 0.4 V up to 1.0 V in steps of 0.1 V and the corresponding power consumption at 27 °C has been listed. The proposed CNTFET FA exhibits 60.32% improvement in Power Consumption when compared to the existing 10 nm FINFET 8-T MGDI Full Adder.

The graphical representation of the effect of power supply variation on the power consumption is depicted in Figure 6. The impact of the variation in the power supply

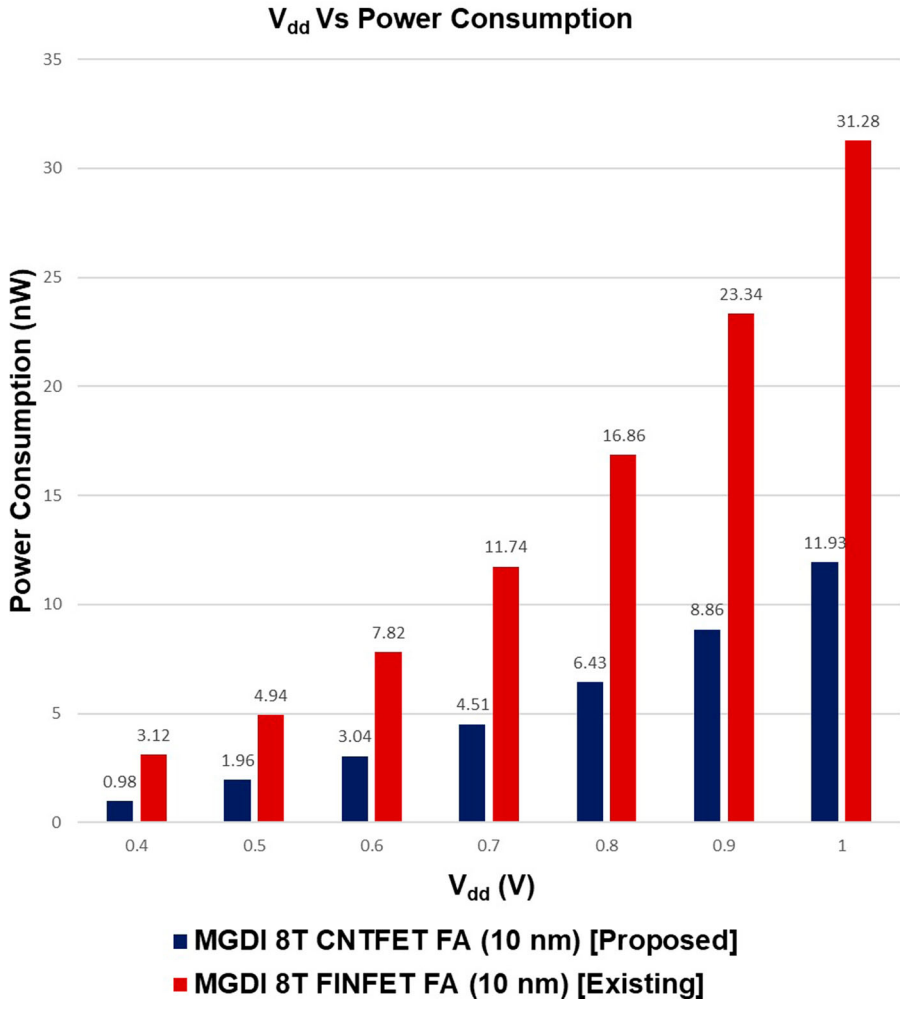

Figure 6: Effect of power supply variations on power consumption

Table 4: Power supply variations vs. propagation delay @ 27°C

Power Supply V_{dd} (V)	8 T MGDI CNTFET FA (10 nm) [Proposed] Propagation Delay (ps)	8 T MGDI FINFET FA (10 nm) [20] Propagation Delay (ps)
0.4	49.57	372.91
0.5	82.63	492.07
0.6	102.51	623.09
0.7	114.05	701.58
0.8	108.41	671.71
0.9	78.23	464.93
1.0	13.01	256.18

on propagation delay of the proposed 8-T MGDI CNTFET FA and the existing 8-T MGDI FINFET FA are listed in Table 4.

The power supply voltage is varied from 0.4 V up to 1.0 V in steps of 0.1 V and the corresponding propagation delay at 27°C has been listed. The Propagation Delay of the proposed FA is 42.16 ps and an improvement of 57.68% has been noticed over the existing FA.

The graphical representation of the effect of power supply variation on the propagation delay is depicted in Figure 7. The impact of the variation in the power supply on PDP of the suggested 8-T MGDI CNTFET-FA and the existing 8-T MGDI FINFET FA is listed in Table 5.

Power supply voltage is varied from 0.4 V up to 1.0 V in steps of 0.1 V and the corresponding power delay product at 27°C has been listed. The PDP of the proposed 10 nm CNTFET 8-T MGDI Full Adder is 82.63×10^{-21} Jules, whereas the PDP of the 10 nm FINFET 8-T MGDI FA is 492.07×10^{-21} Jules. The Power Delay Product of the proposed 10 nm CNTFET 8-T MGDI Full Adder exhibits 83.21% improvement when compared to the 10 nm FINFET 8-T MGDI FA. The graphical representation of the effect of power supply variation on the PDP is shown in Figure 8.

The impact of the variation in the simulation temperature on power consumption of the proposed 8-T MGDI

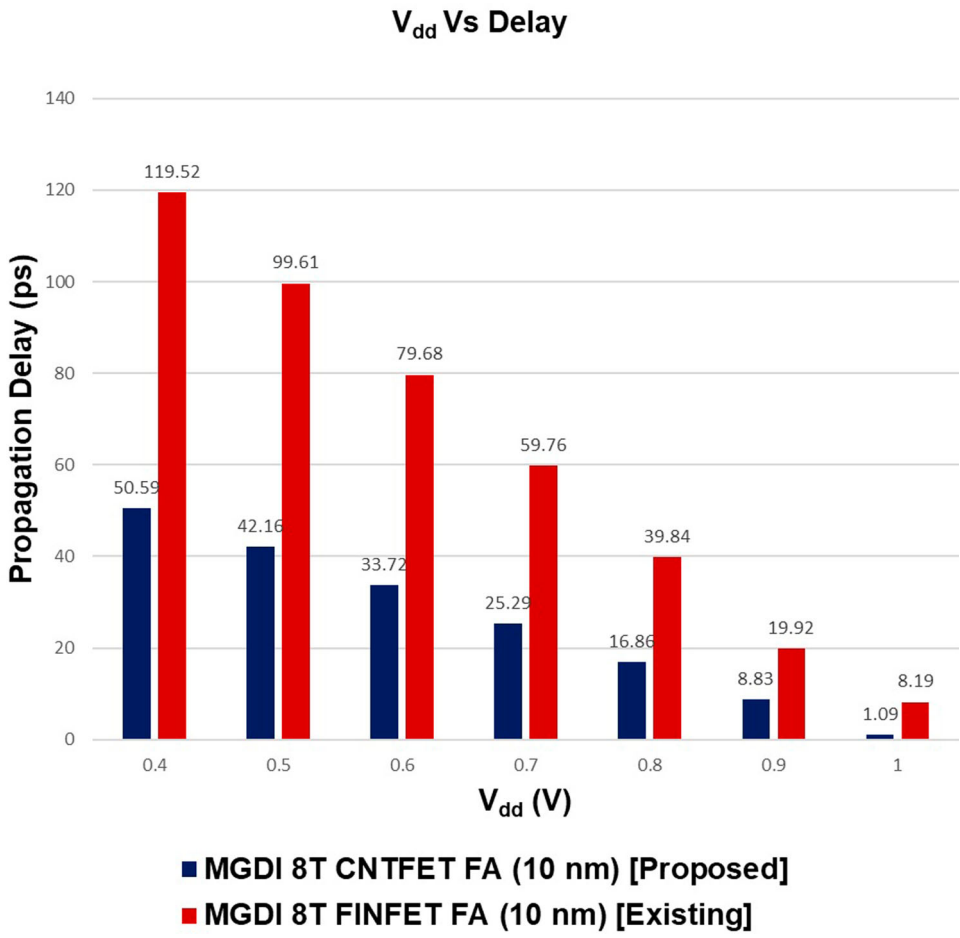

Figure 7: Effect of power supply variations on propagation delay

Table 5: Power supply variations vs. PDP @ 27°C

Power Supply V_{dd} (V)	8 T MGDI CNTFET FA (10 nm) [Proposed] PDP (x10^{-21} Jules)	8 T MGDI FINFET FA (10 nm) [20] PDP (x10^{-21} Jules)
0.4	49.57	372.91
0.5	82.63	492.07
0.6	102.51	623.09
0.7	114.05	701.58
0.8	108.41	671.71
0.9	78.23	464.93
1.0	13.01	256.18

Table 6: Effect of temperature on power consumption @ Vdd = 0.5 V

Temperature (°C)	8 T MGDI CNTFET FA (10 nm) [Proposed] Power (nW)	8 T MGDI FINFET FA (10 nm) [20] Power (nW)
−25	0.42	5.53
0	0.74	6.85
25	1.93	7.71
50	3.29	9.81
75	6.88	13.92
100	10.12	22.15
125	18.82	36.32

CNTFET FA and the existing 8-T MGDI FINFET FA is given in Table 6.

The simulation temperature is varied from −25°C up to +125°C in steps of +25°C and the corresponding power consumption at the power supply voltage of 0.5 V has been given.

The power consumption of the proposed 8-T MGDI CNTFET FA at 27°C is 1.93 nW, whereas the power consumption of the 8-T MGDI FINFET FA at 27°C is 7.70 nW. The proposed 8-T MGDI CNTFET FA exhibits a gradual increment in Power Consumption as the temperature increases, whereas 8-T MGDI FINFET FA Power Consumption increases drastically as the temperature increases and this is exhibited in Figure 9.

The impact of the variation in the simulation temperature on propagation delay of the proposed 8-T MGDI CNTFET FA and the existing 8-T MGDI FINFET FA is given in Table 7. The simulation temperature is varied from −25°C up to +125°C in steps of +25°C and

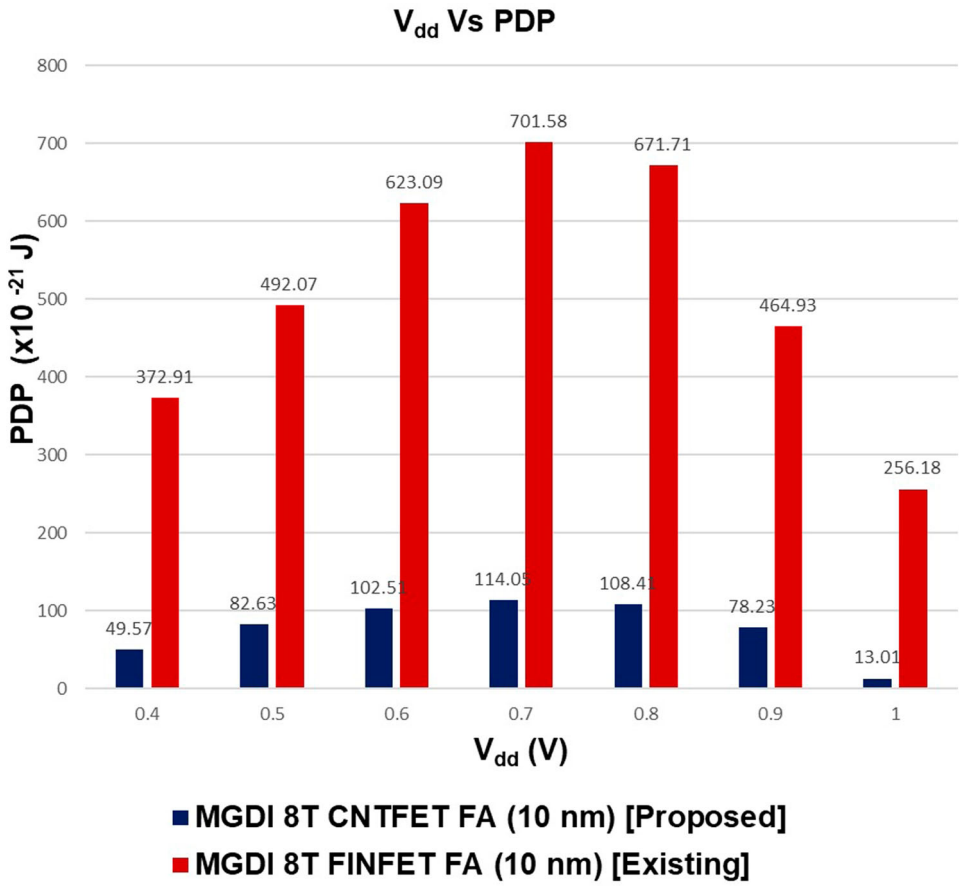

Figure 8: Effect of power supply variations on power delay product

Table 7: Effect of temperature on propagation delay

Temperature (°C)	8 T MGDI CNTFET FA (10 nm) [Proposed] Propagation Delay (ps)	8 T MGDI FINFET FA (10 nm) [20] Propagation Delay (ps)
−25	21.76	47.17
0	32.19	76.21
25	43.94	102.43
50	53.59	128.65
75	67.95	161.41
100	91.36	204.61
125	133.09	264.06

the corresponding propagation delay at the power supply voltage of 0.5 V has been given.

The propagation delay of the proposed 8-T MGDI CNTFET FA at 27°C is 42.16 ps, whereas the power consumption of the 8-T MGDI FINFET FA at 27°C is 99.61 ps. The proposed 8-T MGDI CNTFET FA exhibits a gradual decrement in propagation delay as the temperature increases, whereas 8-T MGDI FINFET FA propagation delay decreases drastically as the temperature increases and this is shown in Figure 10.

The impact of the variation in the simulation temperature on PDP of the proposed 8-T MGDI CNTFET FA and the existing 8-T MGDI FINFET FA is displayed in Table 8. The simulation temperature is varied from −25°C up to +125°C in steps of +25°C and the corresponding PDP at the power supply voltage of 0.5 V has been given. The PDP of the proposed 8-T MGDI CNTFET FA at 27°C is 84.81×10^{-21} J, whereas the PDP of the 8-T MGDI FINFET FA at 27°C is 789.73×10^{-21} J.

4.1 Number of CNT and Diameter Variation

The current characteristics of the CNTFET depend upon the number of the CNTs under the channel. The current flow in the channel is due to the mobile charge carriers in the nanotube channel. The current is directly proportional to the number of tubes. The variation in the CNT number affects the power dissipation and delay of the circuit. For the proposed circuit, the number of tubes is 10. The simulation result variation for power dissipation is done for 2–20 nanotubes.. The simulation variation is shown in Figure 12. The power dissipation of the proposed 8 T MGDI CNTFET FA is 1.96nW for the optimized number of tubes. The simulation shows the gradual increment in the power consumption as the number of tubes increased.

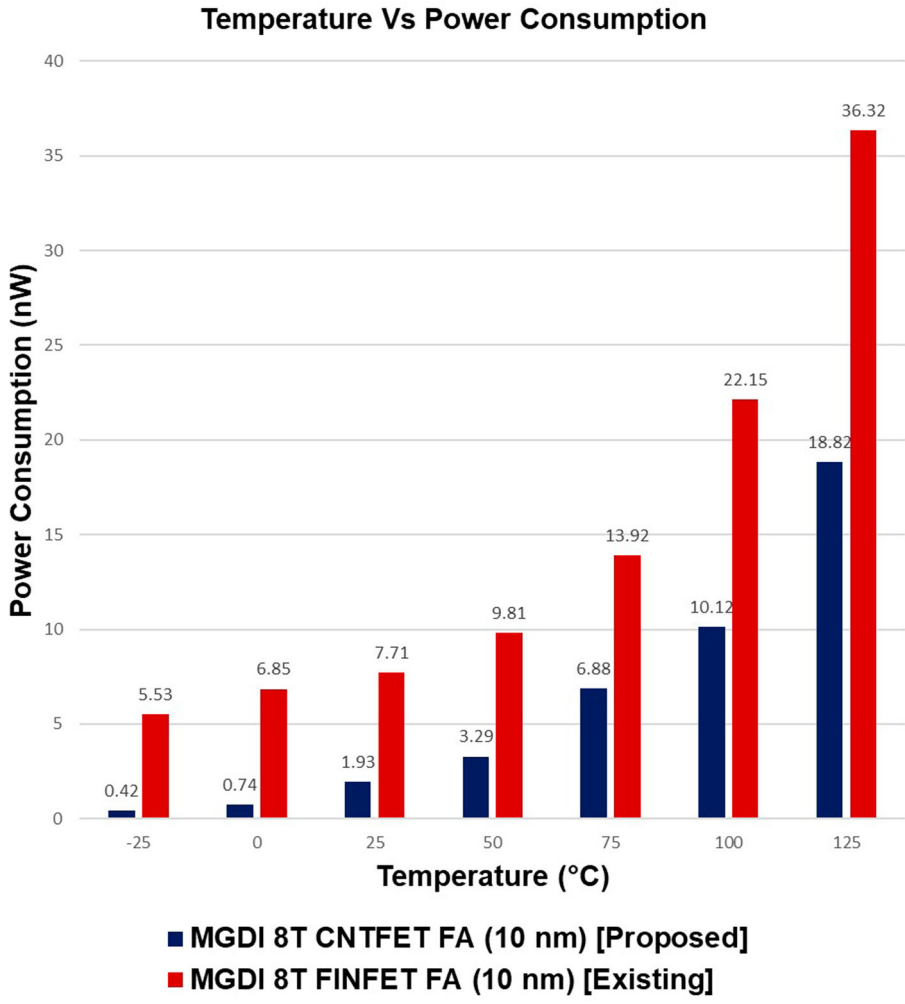

Figure 9: Effect of temperature on power consumption

Table 8: Effect of temperature on power delay product

Temperature (°C)	8 T MGDI CNTFET FA (10 nm) [Proposed] PDP (x10^{-21} Jules)	8 T MGDI FINFET FA (10 nm) [20] PDP (x10^{-21} Jules)
−25	9.76	260.85
0	23.82	522.06
25	84.81	789.73
50	176.31	1262.06
75	467.49	2246.83
100	924.56	4532.11
125	2504.75	9590.66

The propagation delay of the circuit also has an impact on the number of tubes. The variation in the delay with respect to the number of tubes is shown in Figure 13. The delay reduces as the number of tubes increases. The less propagation time will enhance the efficiency of the circuit. For the proposed circuit 8 T MGDI CNTFET FA has 42.16ps delay at 10 nanotubes. It has optimized the value of the propagation time to achieve better performance. The PDP has an effect of the delay and power dissipation. As the number of tubes increases the PDP will decreases. The PDP variation of the Proposed 8 T MGDI CNTFET FA depends upon the number of tubes shown in Figure 14. The PDP of the proposed design is 82.63×10^{-21} joule when the numbers of the tubes is 10 under the CNTFET gate terminal.

The performance of the circuit can be evaluated for different diameters of the CNTs. The diameter is the key component for the CNT performance. The performance of the CNTFET-based adder mostly depends upon the chirality of the CNT. The diameter of the carbon nanotubes depends on the chirality vector [33]. The diameter can be calculated by using the chirality parameter shown in Equation (1) [34].

$$D_{\mathrm{CNT}} = \frac{\mathrm{a}\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.0783\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{1}$$

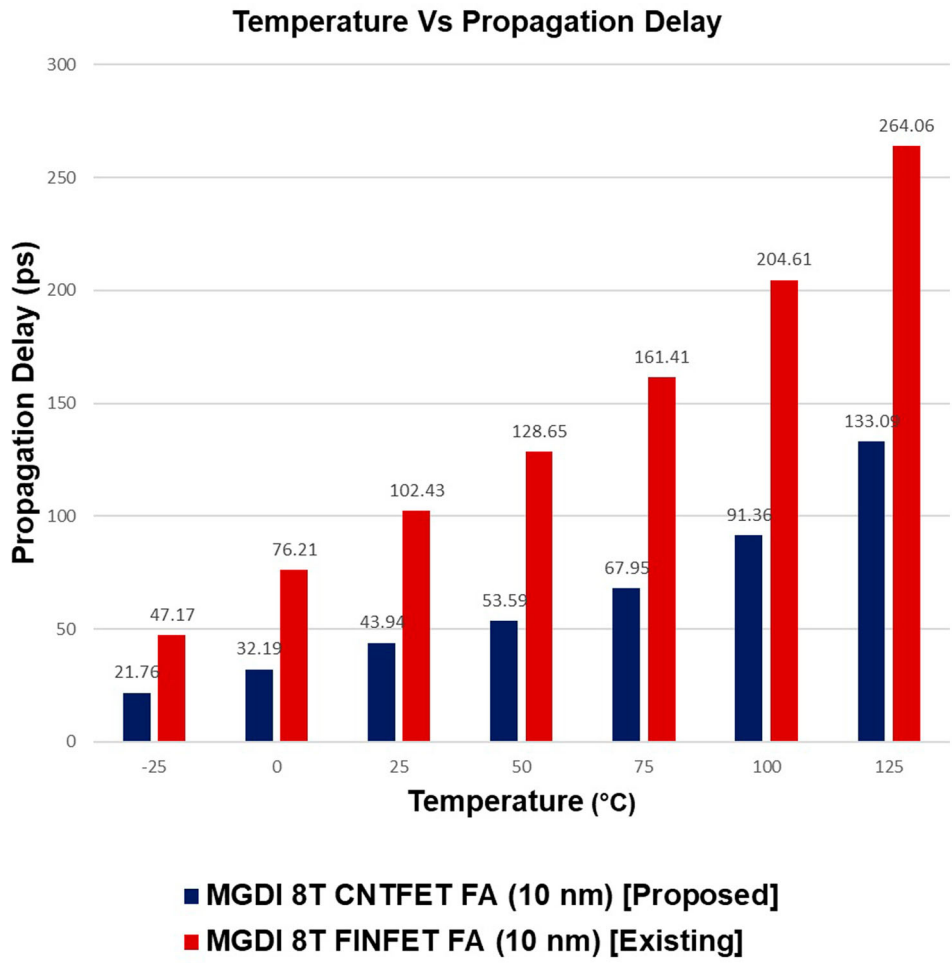

Figure 10: Effect of temperature on propagation delay

n_1 and n_2 are the chirality parameters. These parameters decide the type of the CNTs. The CNT is in metal type if n_1 equals to n_2.

The CNT is a semiconductor if n_1 is not equal to n_2. The threshold voltage of the carbon nanotube depends on the diameter of the CNT. The calculation of the threshold voltage using the diameter is shown in Equation (2).

$$V_{\text{th}} \cong \frac{E_g}{2e} \cong \frac{\sqrt{3}aV\pi}{3eD_{\text{CNT}}} \cong \frac{0.43}{D_{\text{CNT}}} \tag{2}$$

where $a = 2.49$ Å is the atomic distance between two carbon atoms. $V = 3.033$ eV is the carbon π-π bond energy, "e"is the electron unit charge. The current flow in the CNTFET depends upon the threshold voltage of the transistor. The threshold voltage is reducing with the increment in the diameter of the tube. For the CNTFET current flows in the channel are also affected by the diameter of the CNT. The diameter of the CNTs can be varied from 1 nm to 3 nm. The variations are shown for chirality vectors (13,0), (16,0),(19,0), (21,0) and (23,0). The diameters for the given chirality are 1, 1.25, 1.48, 1.64 and 1.8 nm, respectively. The optimized diameter for the proposed design is 1.48 nm which has the chirality vectors (19,0). The variation in the power dissipation due to the diameter is shown in Figure 15. The power is related to the threshold voltage. As the diameter increases the threshold voltage decreases. The power increases gradually with the increment in the diameter. The efficient value of the power can be measured at 1.48 nm diameter tube. The effect of the diameter on the propagation delay is shown in Figure 16. The propagation time has a large impact on the diameter of the nanotubes. The proposed 8 T MGDI CNTFET FA shows that the higher the nanotube diameter, the lesser the propagation delay.

The variation in diameter also affects the power delay product. The PDP is the product of power dissipation and the delay. For the proposed design CNTFET-based design variation is shown in Figure 17.

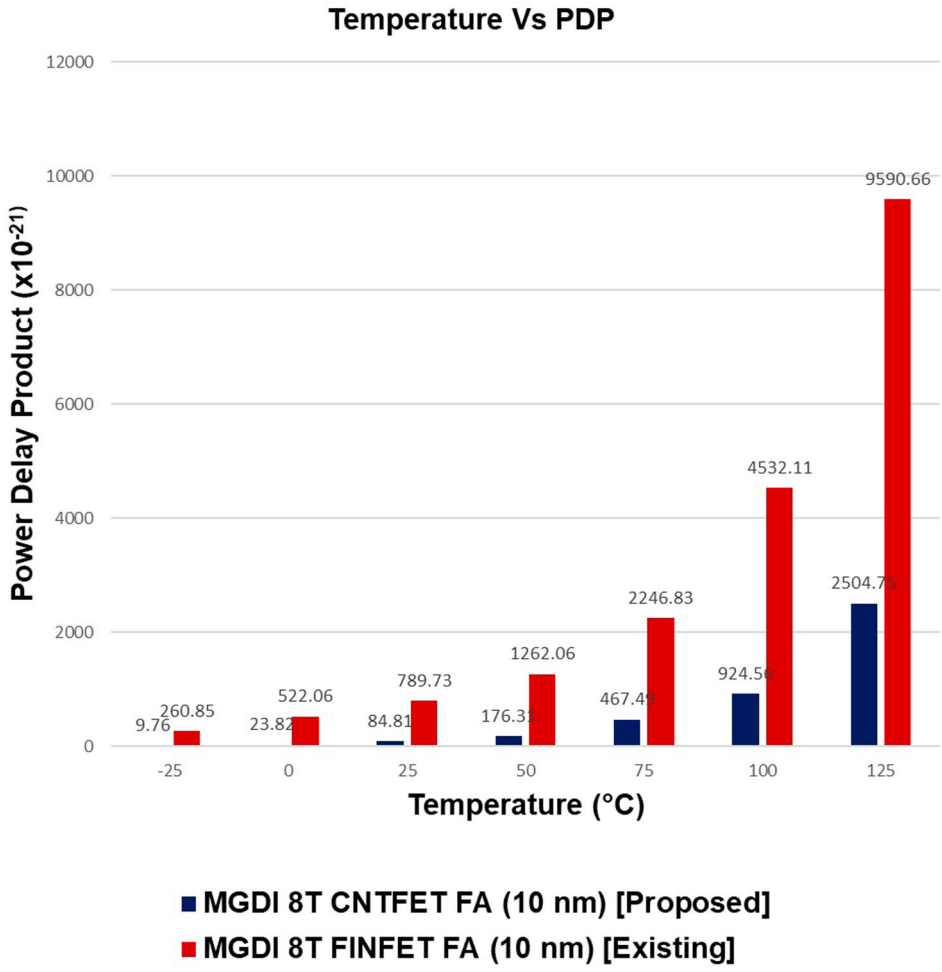

Figure 11: Effect of temperature on power delay product

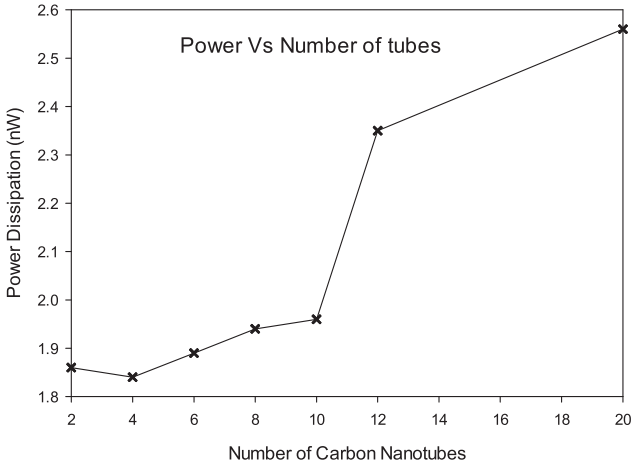

Figure 12: Effect of the number of CNTs on power dissipation

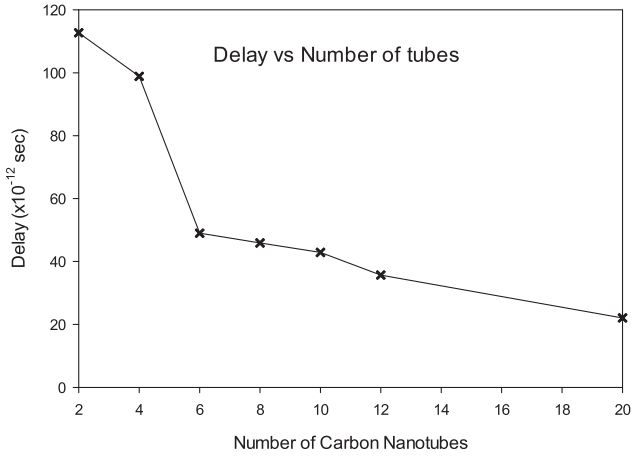

Figure 13: Effect of the number of CNTs on delay

The proposed 8-T MGDI CNTFET FA exhibits a gradual increment in PDP up to 0.7 V as the temperature increases and gradual increment in PDP after that, whereas 8-T MGDI FINFET FA PDP increases drastically up to 0.7 V as the temperature increases and decreases drastically after that and this is shown in Figure 11. The performance metrics of different CNTFET Full Adders have been compared in Table 9. The proposed 10 nm 8-T MGDI CNTFET FA outperforms by means of energy requirement, delay and PDP.

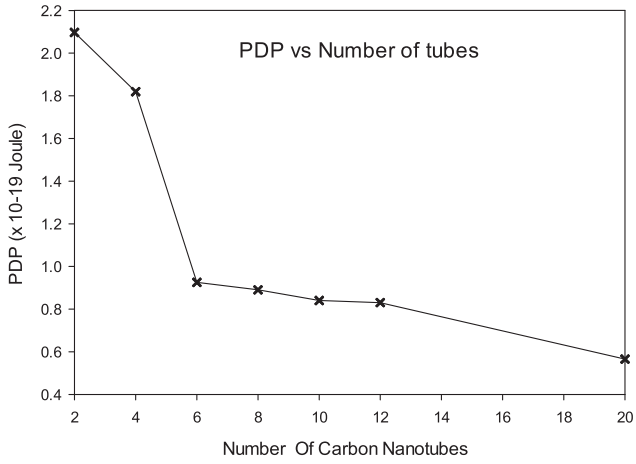

Figure 14: Effect of the number of CNTs on PDP

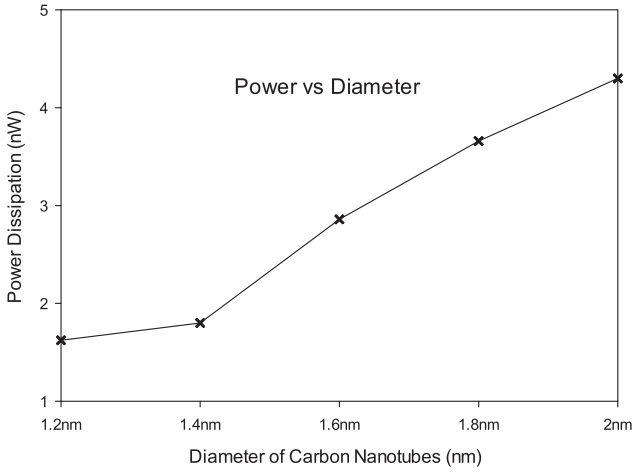

Figure 15: Effect of CNT diameter on power dissipation

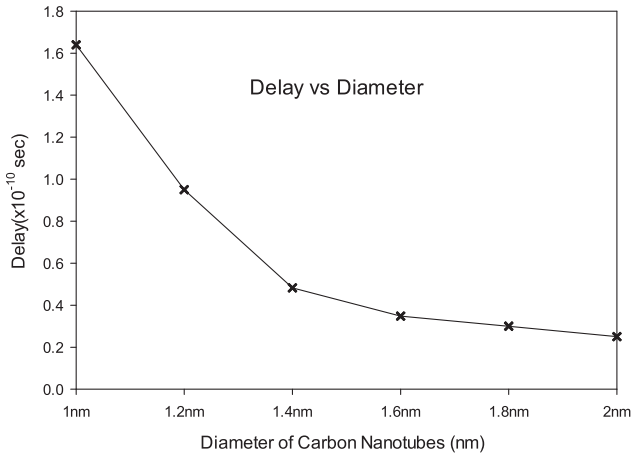

Figure 16: Effect of CNT diameter on delay

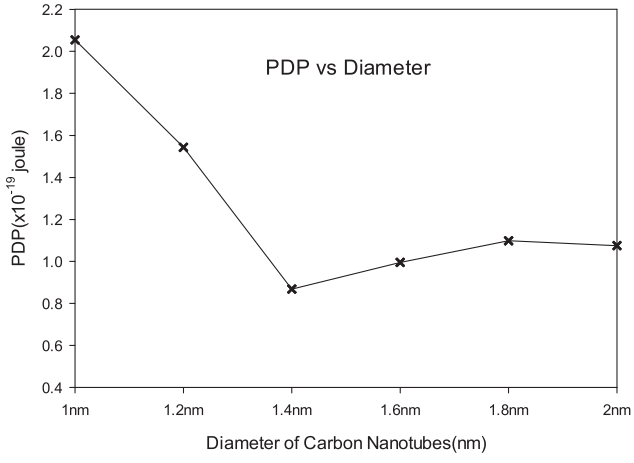

Figure 17: Effect of CNT diameter on PDP

SDTSPC logic-based Fin FET Full adder was implemented for high performance [35]. The main advantage of the SDTSPC logic is that it reduces the problem of charge sharing and noise fluctuation in dynamic logic circuits. The design was implemented by IG-FinFET. This technique was used to reduce the consumption of power and enhance the speed of the circuit. The power consumption of the FinFET full adder was 150.6nW and delay was 196.57×10^{-12} sec for the 0.5volt supply voltage. Over the advantages of the logic the implemented design has a large number of transistors. The implemented design has a large area and high power dissipation in comparison to the proposed MGDI full adder. The 10 T GDI-based FinFET adder was proposed by Pavan *et al.* [36]. It showed the improvement in the performance in comparison to the CMOS design. The power dissipation of the design was 528.9 nW. The delay of sum and PDP was 32.89 psec and17.35×10^{-18} joule for 45 nm node, respectively.

Table 9: Comparison between the proposed designs and other CNTFET full adders

Full Adder	Supply Voltage (Volts)	Number of Transistors	Delay (ps)	Power (nW)	PDP ($x10^{-19}$J)
Design in [30]	0.8	23	14134	1165	164650
Design in [31]	0.5	20	58.8	266	157
Design in [32]	0.8	14	6.39	733	47.15
Design in [33]	0.5	10	1132	2.51	28.3
Design in [24]	0.5	8	89.3	67.39	60.17
Proposed CNTFET (10 nm) Full Adder	0.5	8	42.16	1.96	0.8263

5. CONCLUSIONS

An ultra-low power 8-Transistor MGDI CNTFET-FA has been presented in this paper. Various performance metrics, such as energy requirement, delay and PDP, have

been analyzed with variation in the Power Supply voltage and variation in the Simulation Temperature. The proposed 8-T MGDI CNTFET Full Adder outperforms well by means of energy requirement, delay and PDP at different levels of Power Supply and Temperatures. The power consumption of the proposed 10 nm CNTFET 8-T MGDI Full Adder at 27°C is 1.96 nW. The proposed CNTFET FA exhibits 60.32% improvement in Power Consumption when compared to the existing 10 nm FINFET 8-T MGDI Full Adder. The propagation Delay of the proposed FA is 42.16 ps and an improvement of 57.68% has been noticed over the existing FA. The PDP of the proposed 10 nm CNTFET 8-T MGDI Full Adder is 82.63×10^{-21} Joules, whereas the PDP of the 10 nm FINFET 8-T MGDI FA is 492.07×10^{-21} Joules. The Power Delay Product of the proposed 10 nm CNTFET 8-T MGDI Full Adder exhibits 83.21% improvement when compared to the 10 nm FINFET 8-T MGDI FA.

ACKNOWLEDGEMENT

The author PT is thankful to the officials of AKTU, Lucknow for their continuous support and motivation.

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